Remarks

The Office Action dated October 7, 2008 listed the following rejections: claims 1-3, 15-17 and 19 and stand rejected under 35 U.S.C. § 102(e) over Krivokapic (U.S. Pat. 6,605,843); and claims 12-14 stand rejected under 35 U.S.C. § 103(a) over the '843 reference. Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

All claim rejections are improper and should be removed because the cited '843 reference does not provide correspondence to all of the claim limitations, including those directed to a deep implant layer that prevents source-drain current flow via a parasitic MOS channel. As relevant to the Section 102(e) rejection of each independent claim (1 and 15), the '843 reference fails to show the claimed deep implant layer, per the Office Action's indications that the deep implant layer is "not shown" in the figures. The Office Action then cites to column 1:14-23 in an apparent attempt to show correspondence to the claimed deep implant layer. However, the cited text in column 1 does not describe any deep implant region that prevents the flow of current between a source and drain. Rather, this section appears to discuss conventional p-type and n-type well formation in a silicon wafer, in which subsequent circuit components are formed. The cited well formation makes no mention of preventing any current flow, and the Office Action has provided no explanation as to how the cited well region would do so, or could do so in an operable embodiment. Moreover, the cited text in column 1 does not describe an implant layer that is located between a source and an SOI layer, between a drain and an SOI layer, or separated from a substrate by a SOI layer (*e.g.*, respectively as in claims 2, 3 and 15).

In addition to the above, and referring to cited figures 1-3, it does not appear that any implant region lies between the cited source/drain regions 12/14 and the asserted SOI layer 26, and the implants discussed therein do not prevent current flow as claimed. As the cited source and drain regions are formed directly upon an underlying insulating oxide layer 22 and are separated by a channel region 16, placing a deep implant region between either the source region or the drain region and respective regions 20 of the SOI layer 26 would not prevent any current flow. Correspondingly, placing a deep implant region (as claimed) in the channel region 16 to prevent current flow would render the device inoperable.

Moreover, there does not appear to be any "parasitic MOS channel" via which current would flow, absent a deep implant layer as claimed.

In short, the cited '843 reference is generally unrelated to the claimed invention, and the Office Action has failed to provide correspondence to all claim limitations. As all Section 102 and 103 rejections rely upon the improper assertions regarding the implant layer of independent claims 1 and 15, all rejections are accordingly improper and must be removed.

Further regarding the Section 103 rejection of claims 12-14 over the sole '843 reference, Applicant submits that the rejection is improper because the alleged "routine optimization" of potential, thickness and doping concentration is unsupported by any evidence and fails to disclose the formation of a parasitic MOS channel, from which the claimed implant layer prevents current flow. In alleging that "results" or "purpose" are obvious, the Office Action has also ignored claim limitations such as those directed to the prevention of parasitic current flow, to which the claims are directed. For instance, as is consistent with the specification, the claimed doping concentration is useful for preventing such current flow. Accordingly, the Office Action's unsupported assertions of obviousness not only lack evidentiary support, they are in direct contrast with the instant specification and relevant law relied upon in alleging "routine experimentation." Applicant therefore submits that the Section 103 rejection is also improper for these reasons, and should be removed.

Applicant has made minor amendments to the claims for readability. Applicant has also added new claims, which are believed allowable over the cited reference for reasons including those discussed above, and further because the cited reference does not disclose an implant layer between a source/drain and an underlying silicon-based layer having a parasitic MOS channel therein. Support for these limitations may be found throughout the specification, with exemplary embodiments shown in connection with FIG. 2 and discussion at paragraphs 0010-0014.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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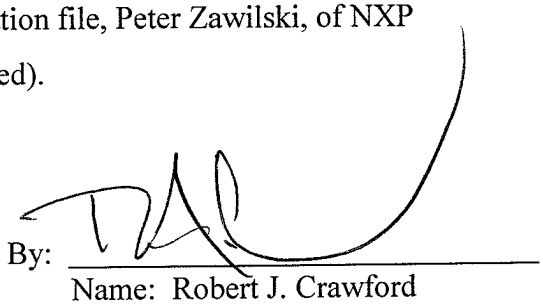
By: 

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